AMENDMENTS TO CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A scan driver with low input voltage, implemented in a flat panel display with a plurality of thin-film transistors (TFTs), the scan driver comprising:

a latch unit, to generate a first control signal and a second control signal, which have opposite phases to each other; and

a level shift circuit, having:

a first switch unit, to receive a first clock signal and a second clock signal, and to perform switching using the first control signal;

a second switch unit, coupled between the first switch unit at both a first connection node and a second connection node and an operating voltage, to receive the first clock signal and the second clock signal through switching the first switch unit, thereby raising voltages at the first connection node and the second connection node to the operating voltage;

a third switch unit, coupled between the first and second connection nodes and the operation voltage, to receive the first control signal and the second control signal through the latch unit, and to receive the first clock signal or the second clock signal through switching the first switch unit, thereby providing a stable processing;

a fourth switch unit, coupled between the first and second connection nodes and the operating voltage, to perform switching of the fourth switch unit according to voltage levels of the first connection node and the second connection node; and

a fifth switch unit, connected to the fourth switch unit, to generate a scan signal to output according to the switching of the fourth switch unit.

2. (Original) The scan driver as claimed in claim 1, further comprising a buffer, connected to the level shift circuit, to receive the scan signal for enhancing driving ability of the scan signal.

3. (Original) The scan driver as claimed in claim 1, wherein the latch unit is an SR latch.

4. (Original) A scan driving system, formed by cascading a plurality of scan drivers, each scan driver comprising:

a latch unit, to apply a set pin and a reset pin respectively to generate a first control signal and a second control signal, which have opposite phases to each other; and

a level shift circuit, having:

a first switch unit, to receive a first clock signal and a second clock signal, and to perform switching using the first control signal;

a second switch unit, coupled between the first switch unit at both a first connection node and a second connection node and an operating voltage, to receive the first clock signal and the second clock signal through switching the first switch unit, thereby raising voltages at the first connection node and the second connection node to the operating voltage;

a third switch unit, coupled between the first and second connection nodes and the operation voltage, to receive the first control signal and the second control signal through the latch unit, and to receive the first clock signal or the second clock signal through switching the first switch unit, thereby providing a stable processing;

a fourth switch unit, coupled between the first and second connection nodes and the operating voltage, to perform switching of the fourth switch unit according to voltage levels of the first connection node and the second connection node; and

a fifth switch unit, connected to the fourth switch unit, to generate a scan signal to an output terminal according to the switching of the fourth switch unit.

5.. (Original) The scan driving system as claimed in claim 4, wherein in the plurality of scan drivers, a set pin of the first scan driver and a reset pin of the last scan driver are connected to a trigger circuit.

6. (Currently Amended) A level shift circuit, comprising:

a first switch unit, to receive a first clock signal and a second clock signal, and to perform switching using ~~the~~ a first control signal;

a second switch unit, coupled between the first switch unit at both a first connection node and a second connection node and an operating voltage, to receive the first clock signal and the second clock signal through switching the first switch unit, thereby raising voltages at the first connection node and the second connection node to the operating voltage;

a third switch unit, coupled between the first and second connection nodes and the operation voltage, to receive the first control signal and ~~the~~ a second control signal, and to receive the first clock signal or the second clock signal through the first switch unit on and off, thereby providing a stable processing;

a fourth switch unit, coupled between the first and second connection nodes and the operating voltage, to perform switching of the fourth switch unit according to voltage levels of the first connection node and the second connection node; and

a fifth switch unit, connected to the fourth switch unit, to generate a scan signal to output according to the switching of the fourth switch unit.

7. (Original) The level shift circuit as claimed in claim 6, wherein each of the first to fifth switch units has a plurality of switching devices.

8. (Original) The level shift circuit as claimed in claim 7, wherein the switching devices are TFTs.